

ABSTRACT OF THE DISCLOSURE

To provide a technique for reducing the power consumption associated with word line activation in a semiconductor memory device. The semiconductor memory device is provided with a word line activation controller for controlling word line activation. Where consecutive operation cycles use multiple-bit addresses that include an identical row address, the word line activation controller can maintain an the activated state of a word line activated during an initial cycle of the consecutive cycles, without deactivating it until a final cycle of the consecutive cycles. If a refresh operation is to be performed during a cycle among the consecutive cycles after the initial cycle, the word line activation controller can deactivate the activated word line prior to performing the refresh operation.